ReRAM Compute ASIC Fabrication

SDDEC24 – 13
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The Problem

Data transfer is commonly bottlenecked between the ALU and memory in intensive circuits limiting the performance.

The Solution

In memory computation is a potential to solve this problem as it stores both data and performs multiplication within the memory resulting in improved processing times and less power consumption.

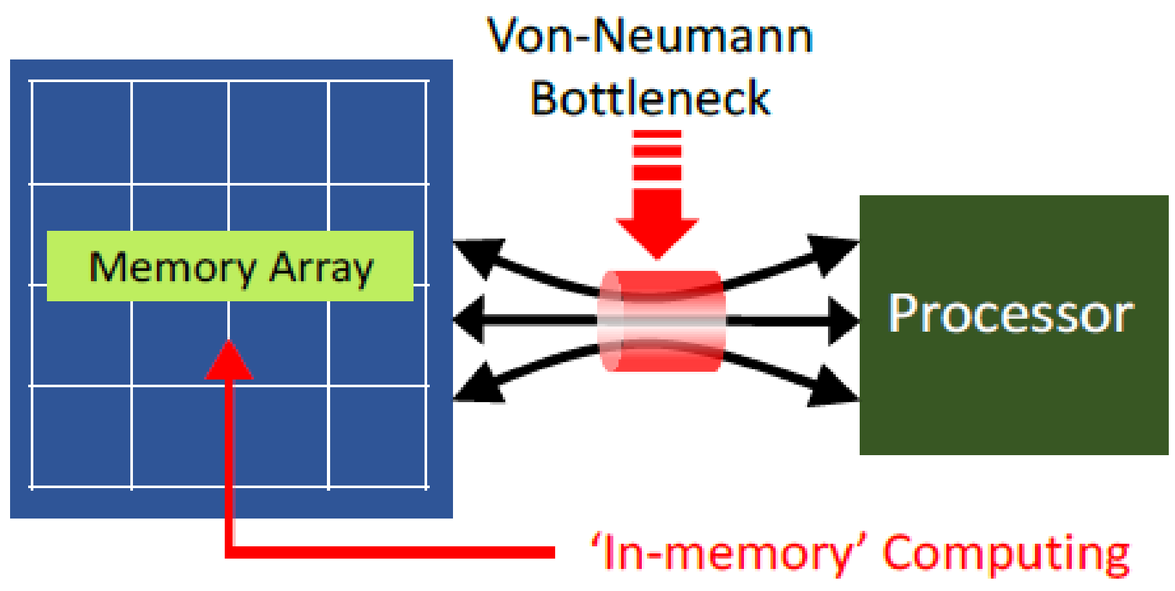

Figure 1 Von Neumann bottleneck

The Users

Users: Dr. Henry Duwe, Dr. Cheng Wang, graduate students, and future senior design teams
Uses: Reasearch into ReRAM for in memory computation, as well as increased knowledge on using the open-source tools

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Design Requirements

- **Functional**
  - Design of an 8x8 crossbar that can perform matrix vector multiplication
  - Design of a peripheral circuitry to control the crossbar
  - Design must fit within 1/8th of the area specified by the eFabless harness (10 mm^2)
- **Nonfunctional**
  - Documentation on tool flows and common issues solved
  - Bring up documentation for testing the design

Concerns and Limitations

- ReRAM crossbar not able to be fully simulated
  - 1T1R cell simulated and verified
  - One directional transistor models hinder crossbar simulation
- Lack of information on noise characteristics could cause ReRAM to act improperly

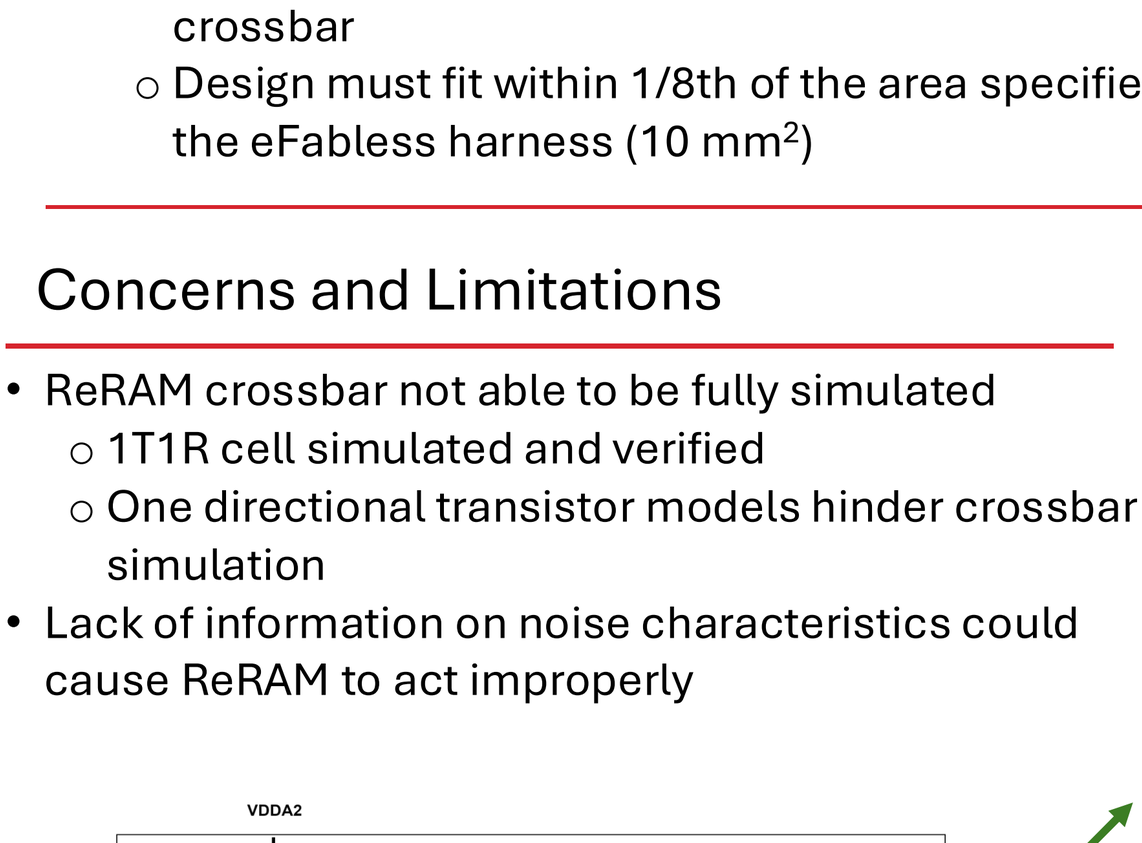

Figure 2 Block diagram of design

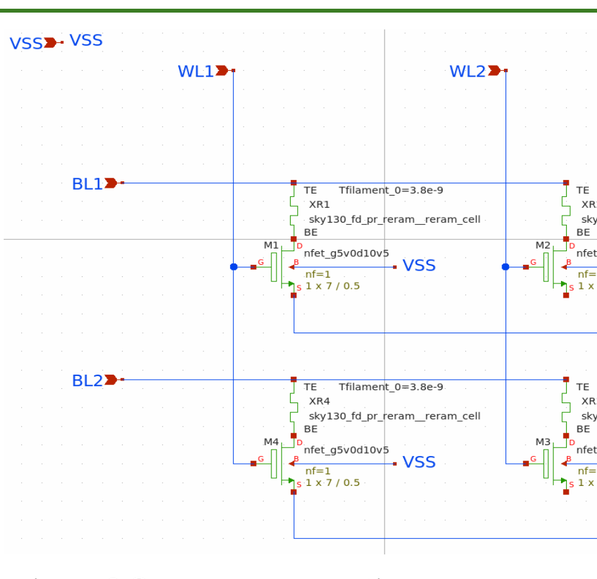

Figure 3 Crossbar schematic

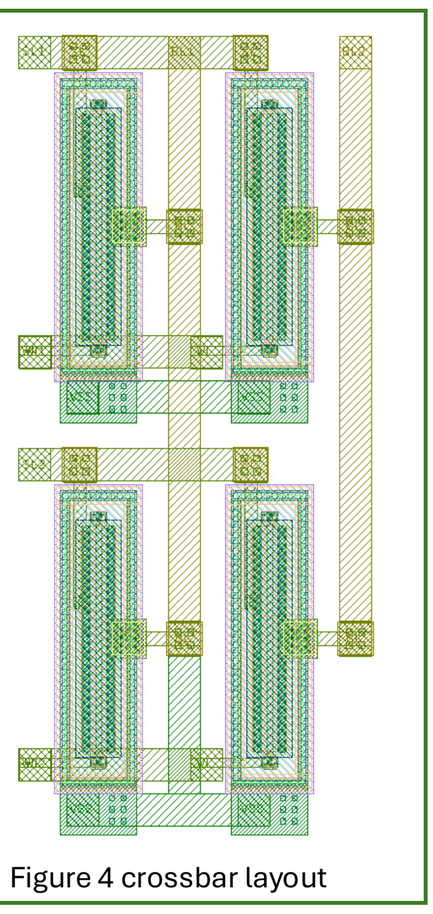

Figure 4 crossbar layout

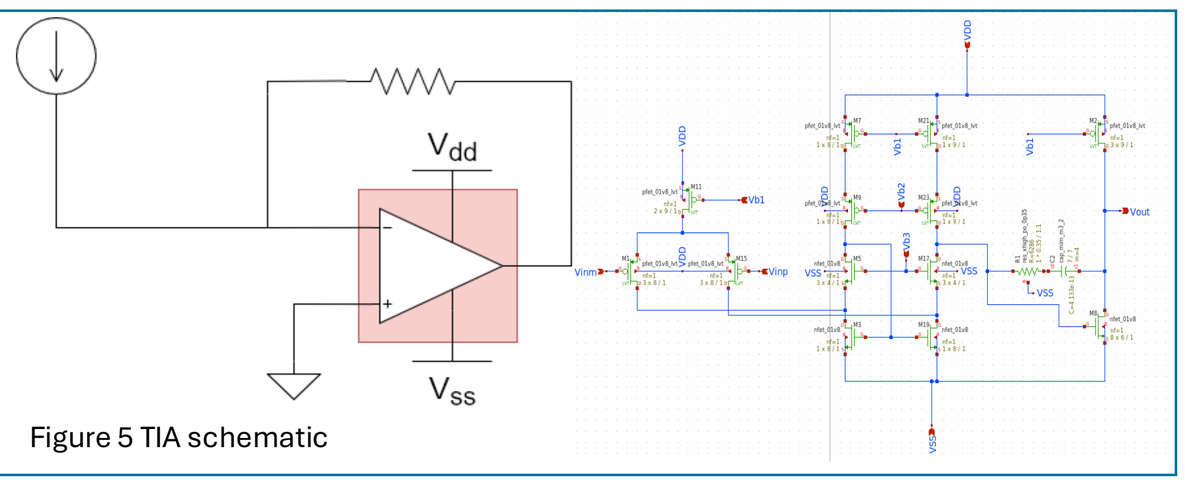

Figure 5 TIA schematic

Figure 6 ADC schematic

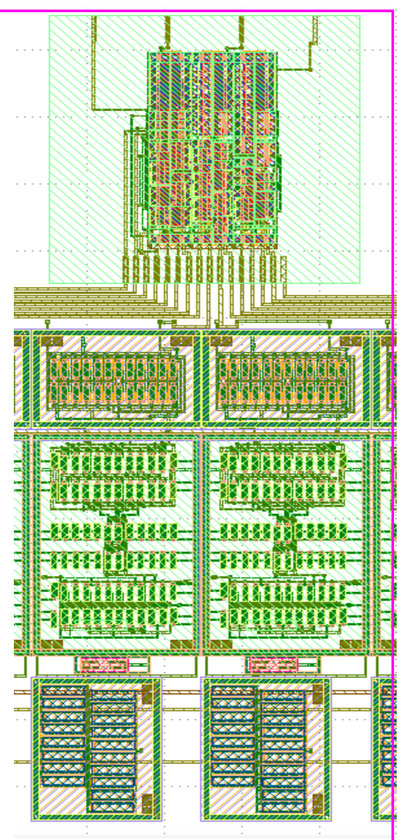

Figure 7 ADC layout

Testing

- Device testing
  - Extensive schematic simulation
  - Characterization of noise
- Results
  - Circuits work as intended and within the design requirements needed